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Title: **JP3273606A2: SEMICONDUCTOR MANUFACTURING SYSTEM**

Country: **JP Japan**

Kind: **A**

Inventor: **HOSOOKA SATORU;**  
**YAGI TORU;**

Assignee: **FUJI ELECTRIC CO LTD**  
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Published / Filed: **1991-12-04 / 1990-09-10**

Application Number: **JP1990000239315**

IPC Code: **H01L 21/02; H01L 21/205; H01L 21/22; H01L 21/68;**

Priority Number: **1990-02-17 JP1990000036583**

Abstract:

**PURPOSE:** To improve throughput considerably and to suppress contamination of wafer considerably by arranging a loading wafer stage and an unloading wafer stage in a first load lock chamber at the opposite sides of a line on one plane, connecting between an atmospheric air carrier and a reaction chamber, and perpendicularly thereto.

**CONSTITUTION:** An atmospheric air carrier 9 takes out a wafer prior to processing and mounts the wafer on a loading wafer stage 24a. A first load lock chamber 18 is then evacuated and the telescoping mechanism of a vacuum carrying robot in a load lock chamber 19 is extended in the direction of the loading wafer stage 24a in order to take out the wafer, which is then loaded in a reaction chamber 3 and subjected to thin film processing. Thereafter, the wafer is mounted on an unloading wafer stage 24b in the first load lock chamber 18. The wafer processed by the atmospheric air carrier 9 is then contained in the original shelf of carrier cassette 10 or 11.

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